

A Wideband Frequency-Shift Keying Wireless Link for Inductively Powered Biomedical Implants

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Abstract—A high data-rate frequency-shift keying (FSK) modulation protocol, a wideband inductive link, and three demodulator circuits have been developed with a data-rate-to-carrier-frequency ratio of up to 67%. The primary application of this novel FSK modulation/demodulation technique is to send data to inductively powered wireless biomedical implants at data rates in excess of 1 Mbps, using comparable carrier frequencies. This method can also be used in other applications such as radio-frequency identification tags and contactless smartcards by adding a back telemetry link. The inductive link utilizes a series-parallel inductive-capacitance tank combination on the transmitter side to provide more than 5 MHz of bandwidth. The demodulator circuits detect data bits by directly measuring the duration of each received FSK carrier cycle, as well as derive a constant frequency clock, which is used to sample the data bits. One of the demodulator circuits, digital FSK, occupies 0.29 mm² in the AMI 1.5- μ m, 2M/2P, standard CMOS process, and consumes 0.38 mW at 5 V. This circuit is simulated up to 4 Mbps, and experimentally tested up to 2.5 Mbps with a bit error rate of 10⁻⁵, while receiving a 5/10-MHz FSK carrier signal. It is also used in a wireless implantable neural microstimulation system.

Index Terms—Biomedical implants, CMOS, data rate, demodulator, inductive coupling, frequency-shift keying (FSK), radio frequency (RF), RF identification (RFID), wireless.

I. INTRODUCTION

AN INDUCTIVE link between two magnetically-coupled coils is now one of the most common methods to wirelessly send power and data from the external world to implantable biomedical devices such as neuromuscular stimulators, cochlear implants, and visual prostheses [1]–[9]. These are not the only applications of data and power transmission via inductive coupling. Radio-frequency identification (RFID), contactless smartcards, and wireless microelectronic mechanical systems (MEMS) are among a few other fields that can highly benefit from this technique, where the use of batteries is avoided due to extreme size, cost, and lifetime constraints [10]–[13]. Achieving high power-transmission efficiency, high data-transmission bandwidth, and coupling insensitivity are some of the major challenges in the design of such systems. Power-transmission efficiency and coupling insensitivity are discussed in [1]–[5]. The focus of this paper is on the high

data-transmission bandwidth and system robustness by making compromises on the power-transmission efficiency.

Some of the biomedical implants, particularly those that interface with the central nervous system, such as cochlear and visual prostheses, need large amounts of data to simultaneously interface with a large number of neurons through multiple channels. It is shown that a minimum of 625–1000 pixels is needed in a visual prosthesis to enable a patient to read text with large fonts [14]–[16]. Every stimulation command in such prosthesis requires 10 bits for addressing the stimulating sites, 6 to 8 bits for stimulation pulse amplitude levels, and 2 to 4 bits for polarity, parity-checking, and sequencing. This would suggest at least 20-bits per command-frame for site selection and stimulus amplitude information. Considering that it might be necessary to stimulate electrodes at rates up to 200 Hz each (for physiological reasons) [17], and the need for four commands per biphasic-bipolar stimulation pulse in our microstimulator architecture [18], raster scanning all 625 sites at this rate requires a serial data bit stream of 625-sites \times 20-bits \times 4-commands \times 200-frames = 10 Mbps. The fact that all the electrodes might not need to be refreshed at all times, significantly reduces the required data rate. However, it is obvious that a high data transmission bandwidth is highly needed for the wireless implantable microstimulator.

In broadband wireless communications such as IEEE-802.11a standard for wireless LAN application, data rates as high as 54 Mbps have been achieved at the expense of increasing the carrier frequency (f) up to 5.8 GHz, yielding a data-rate-to-carrier-frequency ratio of only 0.93%. In other words, each data bit is carried by 107.4 carrier cycles. However, the maximum carrier frequency for biomedical implants is limited to a few tens of megahertz due to the coupled coils self-resonance frequency, increased power loss in the power-transmission circuitry at higher carrier frequencies, and excessive power dissipation in the tissue, which increases as the carrier frequency squared (f^2) [19]. Therefore, the goal is to transmit/receive each data bit with a minimum number of carrier cycles to maximize the data-rate-to-carrier-frequency ratio, and minimize power consumption.

So far, amplitude shift keying (ASK) has been commonly used in the above applications because of its simple modulation and demodulation circuitry [6]–[13], [20]–[22]. This method however, faces major limitations for high-bandwidth data transmission. Because, high-bandwidth ASK needs high order filters with sharp cutoff frequencies, whose large capacitors cannot be easily integrated in this low-frequency end of RF applications. A remedy that has been proposed in the so-called suspended carrier modulation [6], [9], [13], boosts the modulation index up to

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100% (turning the carrier on and off) to achieve high data rates with low-order integrated filters at the expense of an average 50% reduction in the carrier power. Even with this method, data rates above 1 Mbps have not been reported, and they are usually less than 10% of the carrier frequency.

The frequency-shift keying (FSK) modulation scheme is utilized in this work to significantly increase the data transmission bandwidth for wirelessly operating the University of Michigan micromachined stimulating microelectrode arrays that are targeted at 1024 sites for visual and auditory prostheses [23]. Section II introduces the proposed FSK modulation protocol, and compares it with the typical ASK modulation scheme. Section III shows the demodulation circuitry along with simulation results. Section IV describes the design of a wideband inductive link that is developed to support the proposed FSK modulation/demodulation scheme. Section V covers the experimental measurement results, followed by the concluding remarks in Section VI.

II. FSK MODULATION PROTOCOL

FSK is one of the common modulation schemes in digital communication, which simply means sending binary data with a sinusoidal carrier at two frequencies, f_1 and f_0 , representing logic “1” (mark) and logic “0” (space), respectively. Consequently, in the frequency domain, the signal power is centered about these two frequencies, as explained in Section IV (see Fig. 8, **shown later**). The FSK signal can be considered as the summation of two complementary ASK signals $f_0(t)$ and $f_1(t)$ with 100% modulation index. Since $f_0(t)$ and $f_1(t)$ sinusoids usually have the same amplitude, V_m , an excellent characteristic of the FSK modulation for inductively powered wireless devices is that the transmitted power is always constant at its maximum level, irrespective of f_0 , f_1 , frequency modulation index, or the data contents

$$|f_0(t)| = |f_1(t)| = V_m \Rightarrow P_{\text{rms}}(\text{FSK}) = \frac{1}{2}V_m^2 = \text{const.} \quad (1)$$

This would allow a further relative distance between the receiver and transmitter coils (d_r) or a smaller transmitted power, which is important since the maximum allowable tissue exposure to electromagnetic power is limited in biomedical devices [19]. Conversely, the power fluctuations due to ASK modulation impose additional power regulation and filtering challenges, especially when the modulation index is high [12].

The superior robustness against various noise sources and interference of FM over AM has been known since the early stages of radio engineering. This fact is even more significant in inductively powered devices, most of which receive data and power from the same carrier. When all other parameters are constant, the induced voltage across the receiver coil is inversely proportional to the third power of the coils relative distance ($1/d_r^3$) [1]. This means that the induced signal amplitude, which is the information carrying entity in ASK systems, is extremely sensitive to d_r , and is prone to patient movements (motion artifacts) in biomedical implants, or hand vibrations in RFID tags and smartcards. Even when d_r is constant, since the received power

is also constant ($V \times I$), any changes in the wireless chip current consumption, due to digital circuitry current impulses for example, directly results in the received carrier envelope voltage variations, and deteriorates the quality of the ASK signal [12]. In FSK systems on the other hand, it is very unlikely that d_r or current variations would affect the frequency of the induced signal.

In ASK modulation, the transmitter and receiver inductive-capacitive (LC) tank circuits should have high quality factors (Q), tuned at the carrier frequency to get enough amplitude variations (gain) for data detection as well as high power-transmission efficiency ($\eta \leq 40\%$) [1]–[5]. In the proposed FSK modulation protocol however, the wireless link pass-band contains both f_0 and f_1 with a low Q to transfer enough energy at both carrier frequencies at the expense of a lower power-transmission efficiency (see Figs. 9 and 11, **shown later**). This can be another advantage for the FSK technique, because in the applications of interest the quality factor of the miniature receiver coil is inherently low, particularly when the receiver coil is integrated, and its high resistivity is unavoidable [11], [20]. Therefore, the ASK systems not only lose the power efficiency advantage but also the data bandwidth, while the FSK systems can still maintain a high bandwidth for data transmission.

Synchronization of the receiver with the transmitter, though, is easier in ASK systems. The implant or RFID internal clock signal can be directly derived by stepping down the constant ASK carrier frequency [11], [12], [20]–[22]. In phase-coherent FSK, where the carrier frequencies (f_0 and f_1) have a fixed phase at the onset of every bit, an internal clock with a constant frequency can be derived from a combination of the two carrier frequencies based on the FSK modulation protocol. In noncoherent FSK, where the carrier phase is random, the timing information should be encoded within the data bit-stream by using self-clocking schemes such as Manchester or Miller [24]. The first option was utilized in the proposed FSK protocol with a non-return-to-zero (NRZ) data bit-stream to achieve a higher data rate.

To maximize the data-rate-to-carrier-frequency ratio, a phase-coherent protocol was devised for the FSK data transmission with data rates as high as f_1 , where f_0 is twice as f_1 . In this protocol, logic “1” is transmitted by a single cycle of the carrier f_1 , and logic “0” is transmitted by two cycles of the carrier f_0 , as shown in Fig. 1. The carrier frequency switches at a small fraction of a cycle and only at negative-going (or positive-going) zero crossings. This leads to a consistent bit length of $1/f_1$, and maximum data rate of f_1 bits per second. As a result, if the average carrier frequency is considered to be $f_{\text{avr}} = (f_0 + f_1)/2$, then the data-rate-to-carrier-frequency ratio can be as high as 67%. It is also notable that any odd number of consecutive f_0 cycles in this protocol is an indication of data transmission error.

Either active or passive reverse telemetry can be used in any of the aforementioned applications to send information back from the wireless chip to the transmitter. In the active reverse telemetry, a transmitter with a separate antenna, which usually works at a higher frequency, is implemented on-chip. In passive reverse telemetry, the receiver coil loading (load modulation) or capacitive tuning (resonant frequency shifting) is changed based

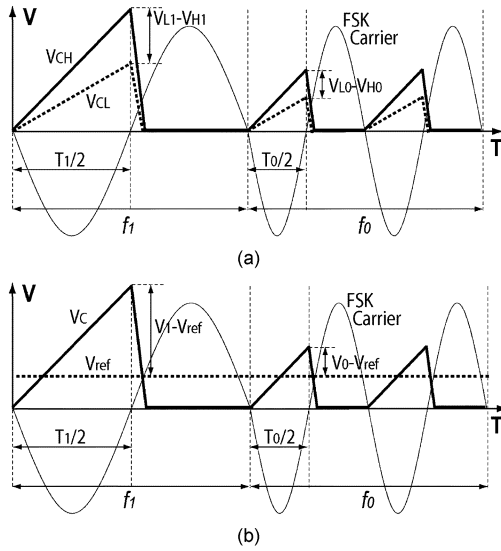


Fig. 1. Proposed phase-coherent FSK modulation protocol and analog FSK data detection techniques. (a) Fully Differential FSK [25]. (b) Referenced Differential FSK [26].

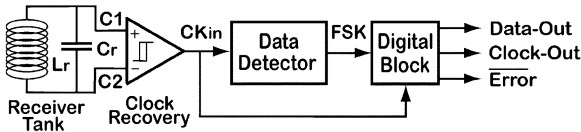


Fig. 2. Block diagram of the FSK demodulator.

on the feedback information, and the effects of these changes are sensed at the transmitter coil [10]. Using the carrier frequency variations for forward data transmission facilitates use of the carrier amplitude variations for reverse telemetry. Reverse telemetry is out of the scope of this paper, however, any of the above methods can be incorporated with the proposed FSK modulation technique to provide a half- or full-duplex communication between the two parts of a wireless system.

III. FSK DEMODULATION CIRCUITS

Common FSK demodulation techniques such as FM discriminator, phase locked loop, or quadrature detector circuits need some kind of analog filtering down the signal path, which would consume a large chip area in the low-end RF applications of interest. Therefore, the received FSK carrier was treated as a base-band signal to eliminate any type of mixing or filtering. The data detection technique used here for FSK demodulation is based on measuring the period of each received carrier cycle, which is the information carrying entity in FSK modulation scheme. If the period is higher than a certain value, a logic “1” bit is detected, and otherwise a logic “0” bit is received. Fig. 2 shows the FSK demodulator block diagram. A clock recovery (or regenerator) block squares up the sinusoidal carrier across the receiver $L_r C_r$ -tank circuit (CK_{in}), and feeds it into the data detector block, which discriminates between the short (f_0) and long (f_1) carrier cycles. Finally, a digital block recovers the received serial data bit-stream as well as a constant frequency clock to sample the data bits.

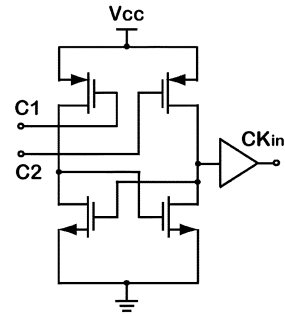


Fig. 3. Schematic diagram of the clock regenerator.

A. Analog FSK Demodulation

A simple method for time measurement in analog circuits is charging a capacitor with a constant current and monitoring its voltage. In the FSK demodulator, charging and discharging of this capacitor should be synchronized with the FSK carrier signal. If the capacitor voltage is higher than a certain value, a logic “1” bit is detected and otherwise a logic “0” bit is received. This comparison can be done in two ways.

- 1) *Fully differential FSK (FDFSK) demodulator*: Charging two unequal capacitors with different currents, and comparing their voltages by a hysteresis comparator as shown in Fig. 1(a) [25].
- 2) *Referenced differential FSK (RDFSK) demodulator*: Charging a single capacitor, and comparing its voltage with a constant reference voltage as shown in Fig. 1(b) [26].

Fig. 3 shows the clock recovery circuit, which is a cross-coupled differential pair, directly connected to the $L_r C_r$ -tank nodes (C_1 and C_2), as shown in Fig. 2. Utilization of a positive feedback in this circuit helps generating sharp output CK_{in} edges, which are necessary for precise timing of the carrier cycles. Fig. 4(a) shows a simplified schematic diagram of the FDFSK data detector circuit. When CK_{in} is low, S_L and S_H switches are open and S_{LC} and S_{HC} are closed. Therefore, the current sources I_L and I_H linearly charge C_L and C_H up to V_L and V_H , respectively. During a logic “1” long cycle, V_{L1} and V_{H1} are twice as V_{L0} and V_{H0} when a logic “0” short cycle is being received, because in the phase-coherent FSK protocol in Fig. 1(a), T_1 is twice as T_0 . A hysteresis comparator compares capacitor voltages. The hysteresis window width, W_{hyst} , is set somewhere between $V_{H1}-V_{L1}$ and $V_{H0}-V_{L0}$. Therefore, the comparator output switches to high during a logic “1” long cycle but not during a logic “0” short cycle. S_L and S_H switches discharge the capacitors in a fraction of the FSK 2nd half cycle, when CK_{in} is high. Meanwhile, S_{LC} and S_{HC} switches open to halt I_L and I_H , and reduce power consumption. CK_{in} also resets the hysteresis comparator to be ready for the next carrier cycle.

Fig. 4(b) shows a simplified schematic diagram of the RDFSK demodulator, which is the single-ended equivalent of the FDFSK. When CK_{in} is low, I_C linearly charges the capacitor C . During a logic “1” long cycle, C is charged up to V_1 , which is twice as V_0 when a logic “0” is received. A hysteresis comparator, with W_{hyst} between V_1-V_{ref} and V_0-V_{ref} , compares the capacitor voltage with a constant 1.26 V bandgap

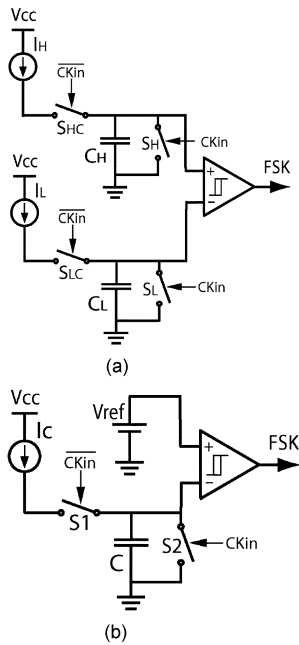


Fig. 4. Simplified schematic diagrams of (a) FDFS and (b) RDFS data detector circuits.

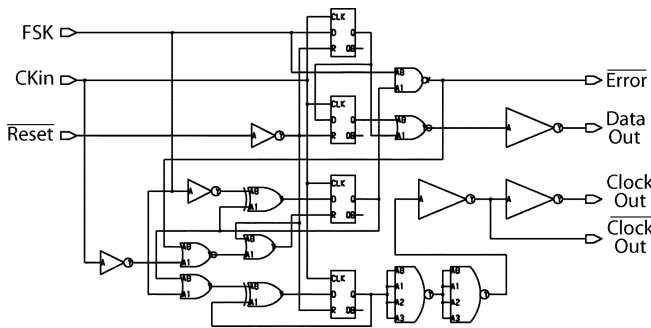


Fig. 5. Schematic diagram of the digital block.

reference. The comparator output switches to high during logic “1” but not logic “0”. Finally, S_2 discharges C in a fraction of the carrier second half cycle, when CK_{in} is high, meanwhile, S_1 opens to reduce power consumption by halting I_C .

The output of the FDFS or RDFS data detector blocks, called FSK, is only a series of pulses, which discriminate between long and short FSK carrier cycles. Thus, it cannot be directly regarded as the received data bit-stream. These pulses are fed into a digital block, shown in Fig. 5, along with CK_{in} to generate the serial data output (*Data-Out*) and constant frequency clock (*Clock-Out*). On every rising edge of the CK_{in} , a 2-bit shift register shifts in the status of the FSK signal. Every 2 successive short cycles should be regarded as a “0” bit on *Data-Out*, and every single long cycle indicates a “1” bit. Any odd number of short cycles is an indication of error according to the FSK protocol, and activates the error flag (*Error*). To generate a constant frequency clock, a T flip-flop indicates the number of successive zeros, and another T flip-flop toggles on every long CK_{in} cycle or two successive short CK_{in} cycles. The resulting clock frequency is constant at $f_1/2$ irrespective of the data contents. Digital block is designed asynchronously to minimize the number

of gates and consequently the circuit area, as well as desensitize it to CK_{in} or *Clock-out* timing jitter. Therefore, signal propagation and timings were considered carefully, and delay elements were added, before the *Clock-Out* buffer for example, to avoid metastable operation of the following digital circuitry that are supposed to sample and decode the serial data bit-stream [18].

B. Digital FSK Demodulation

In a digital approach for FSK demodulation, the duration of the carrier cycles are measured with a constant-frequency clock time-base (f_{TB}) at a rate several times higher than the carrier frequencies (f_0 and f_1) [27]. Most often, f_{TB} , which does not need to be synchronized with the carrier, is already available in the system for running other digital blocks such as a microcontroller. An n -bit counter runs while the carrier is “positive” and measures half of a carrier cycle. When the carrier goes “negative”, the counter stops, and a digital comparator decides whether a long or short carrier cycle is received by comparing the count value with a constant reference number. Then it resets the counter for measuring the duration of the next cycle.

It is necessary for the time-base period ($1/f_{TB}$) to be smaller than the time-difference between f_0 and f_1 half-cycles to enable the demodulator to discriminate between these two frequencies. In other words, f_{TB} should be

$$f_{TB} > \frac{2f_1f_0}{f_0 - f_1} \quad (2)$$

In addition, the minimum width of the counter (n) should satisfy

$$2^n > f_{TB}/f_0. \quad (3)$$

In order to simplify the demodulator circuit, and reduce dynamic power consumption, the digital comparator can be combined with the counter by choosing f_0 , f_1 , f_{TB} , and n such that

$$f_0 > f_{TB}/2^n > f_1 \quad (4)$$

In this case, the most significant bit (MSB) of the counter determines whether a long or short carrier cycle is received, and the constant reference number would be 2^n .

Based on the proposed FSK modulation protocol, fabrication process parameters, and required bandwidth for a visual implant, f_0 and f_1 were chosen equal to 8 and 4 MHz, respectively. A lower limit for the time-base clock, $f_{TB} > 16$ MHz, is set by (2). By choosing $n = 3$, (4) defines a new range for f_{TB} , $64 \text{ MHz} > f_{TB} > 32 \text{ MHz}$, which satisfies (2) and (3) as well. Therefore, a 5-stage ring-oscillator was designed to generate $f_{TB} = 49 \text{ MHz}$ at the center of the above range to provide the maximum level of robustness. It should be noted that as long as f_{TB} is in the desired range, the phase noise and process- or temperature-dependent frequency variations of the ring oscillator do not affect the demodulator performance.

Fig. 6 shows the schematic diagram of the DFSK demodulator, and Fig. 7 shows sample simulation waveforms when “00111100110011” data bit-stream {trace-1} is FSK modulated and applied to the DFSK demodulator circuit {2}. The clock recovery block squares up the received FSK carrier, and generates CK_{in} {3}. The 5-stage ring-oscillator generates f_{TB} at 49 MHz,

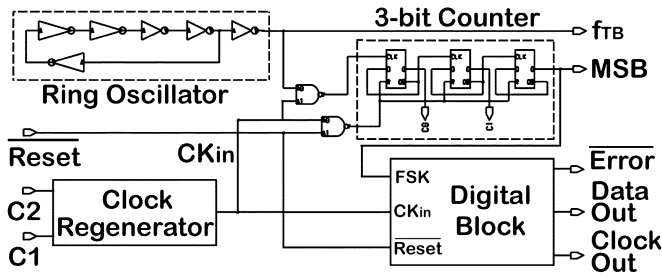


Fig. 6. Schematic diagram of the DFSK demodulator.

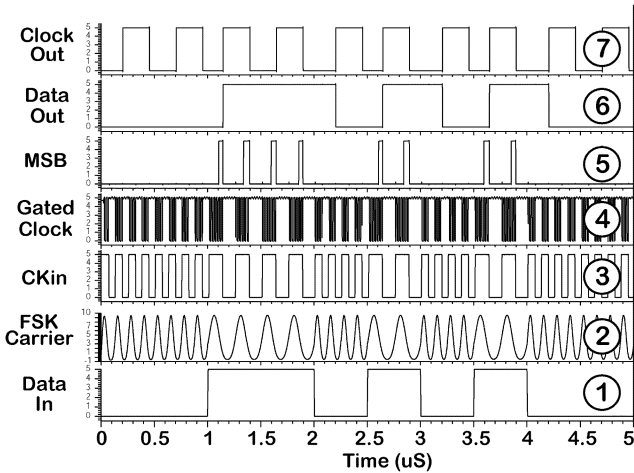


Fig. 7. Simulated waveforms of the DFSK demodulator.

which runs the 3-bit counter after being gated by $CK_{in}\{4\}$. When CK_{in} is high, the counter is running, and it resets when CK_{in} is low. The counter MSB stays low during short (62.5 ns) carrier half-cycles when $count < 4$, however, it goes high during long (125 ns) carrier half-cycles when $count \geq 4$ {5}. The counter resets during the 2nd carrier half-cycle to be ready for detecting the type of the next cycle. The MSB signal {5} cannot be directly regarded as the received serial data bit-stream. Therefore, these pulses are fed into the digital block (Fig. 5) along with $CK_{in}\{3\}$ to generate *Data-Out* {6} and *Clock-Out* {7}.

IV. WIDEBAND INDUCTIVE LINK

A. Required Bandwidth

Detailed design of the inductive link for biomedical implants can be found in [1]–[5]. All of these inductive links, except for [5], are designed to maximize the gain and power-transmission efficiency of the link at the expense of a narrow bandwidth by using high- Q LC tanks, tuned at the carrier frequency, on both transmitter and receiver sides. Therefore, they are only suitable for narrowband ASK carriers, which is not the case in the proposed FSK modulation scheme. Carlson's rule approximates the bandwidth (BW) needed to include 98% of the total power of an FM signal [24]:

$$BW \approx 2(\delta_{\max} + f_{i\max}) \quad (5)$$

where δ_{\max} is the maximum frequency shift caused by modulation, and $f_{i\max}$ is the maximum frequency content of the modulating signal. In the proposed FSK protocol, $\delta_{\max} = f_1/2$ with

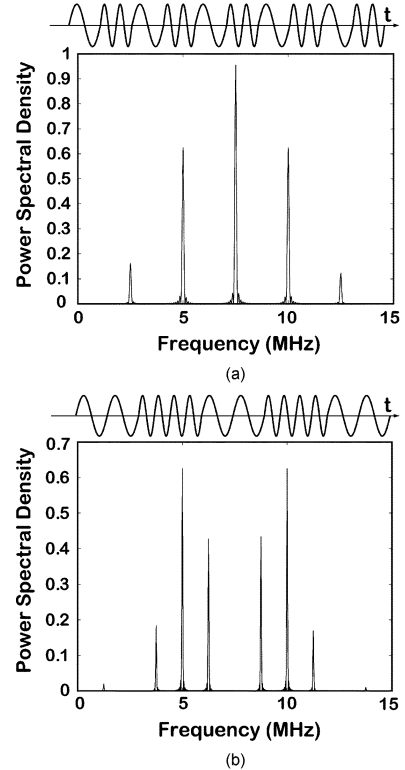


Fig. 8. Simulated power spectral density of the proposed phase-coherent FSK carrier at $f_1 = 5$ MHz and $f_0 = 10$ MHz. (a) The widest required bandwidth when each bit is repeated once: $BW \approx 10$ MHz for 5 Mbps. (b) The widest required bandwidth when each bit is repeated twice: $BW \approx 7.5$ MHz for 2.5 Mbps.

respect to f_{avt} , and the maximum data rate of f_1 (bps) can be considered as a square modulating signal at $f_1/2$. Therefore, the main lobe of the modulating signal spectrum has a maximum frequency of $f_{i\max} = f_1$. By substituting these values in (5), a bandwidth of $BW \approx 3f_1$ is needed to include 98% of the FSK carrier power. It should be noted, however, that contrary to the analog FM, here the goal is not a direct reconstruction of the square data waveform, but correct detection of the data bits. Hence, depending on the application, a smaller bandwidth might be still adequate to provide an acceptable bit error rate (BER), even though it lowers the power-transmission efficiency, due to less than 98% spectral coverage. Fig. 8 shows the simulated power spectral density of the proposed phase-coherent FSK carrier at $f_1 = 5$ MHz and $f_0 = 10$ MHz. Fig. 8(a) shows the widest required bandwidth at 5 Mbps when 1010101... is transmitted, and each bit is repeated only once ($BW \approx 10$ MHz). A 25% reduction in the required bandwidth can be achieved by repeating every bit twice, 1100110011..., at the expense of a 50% reduction in the actual data rate to 2.5 Mbps, as shown in Fig. 8(b) ($BW \approx 7.5$ MHz).

B. Inductive Link Topology and Design

The easiest way to increase the inductive link bandwidth is to lower the Q of the carrier frequency tuned LC tank circuits of [1]–[4] by adding resistive components. However, the resulting increase in power dissipation is not desirable. The stagger-tuning technique, proposed in [5], was tried in simulations by tuning the transmitter and receiver LC tanks at

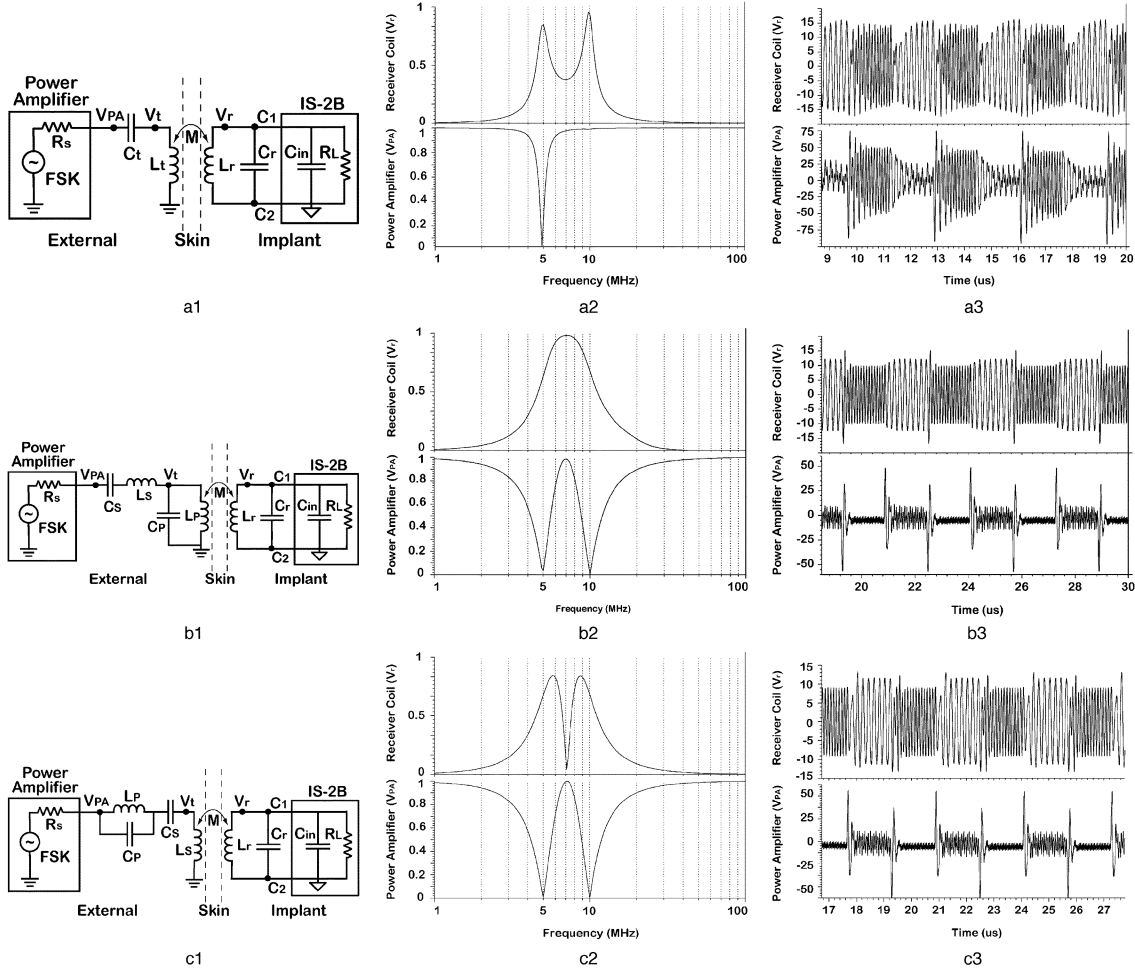


Fig. 9. (1) Simplified schematics, (2) frequency-domain spectrums, and (3) time-domain waveforms of three wideband inductive links for the phase-coherent FSK data and power transmission at $f_1 = 5$ MHz and $f_0 = 10$ MHz. (a) Stagger-tuning at f_0 and f_1 . (b) Series-parallel LC tank combination with L_P as the transmitter coil. (c) Series-parallel LC tank combination with L_S as the transmitter coil. V_{PA} : Power amplifier output voltage V_r . Voltage across the receiver coil. Component values for (b) and (c) are listed in Table I.

f_1 and f_0 , respectively, as shown in Fig. 9(a). In these simulations, the external transmitter (power amplifier) is represented by an ac voltage source with output resistance R_s , whereas the biomedical implant is replaced by a resistive load (R_L) and its parasitic input capacitance (C_{in}). Fig. 9 rows from top show the circuit schematics, frequency-domain spectrums (normalized to eliminate the effect of d_r), and time-domain waveforms across the transmitter output (V_{PA}) and receiver coil (V_r) for three wideband inductive links. The main problem with the stagger-tuned link for this application is the ISI, shown in Fig. 9(a3), which is caused by the residual ringing that distorts V_r when the transmitter switches from one frequency to another. The residual ringing, which is due to the high Q of the LC tanks, could be reduced by moving the resonance frequencies further apart, provided that they are still well below the receiver coil self-resonance frequency.

Another option is using a combination of both series and parallel LC tank circuits to reshape V_r spectrum by modifying the V_{PA} frequency response with adding two zeros at f_0 and f_1 , where the peaks of the FSK carrier spectrum are located (see Fig. 8). Fig. 9(b) and (c) shows simplified schematic diagrams of the modified inductive link. It can be analytically shown that

this condition will be satisfied if L_S-C_S and L_P-C_P are chosen such that

$$\frac{1}{2\pi\sqrt{L_P C_P}} = \frac{1}{2\pi\sqrt{L_S C_S}} = \sqrt{f_0 f_1} = f_r \quad (6)$$

$$\frac{1}{2\pi\sqrt{L_S C_P}} = f_1 \quad (7)$$

$$\frac{1}{2\pi\sqrt{L_P C_S}} = f_0 \quad (8)$$

The effect of L_r and its loading (C_r , C_{in} , and R_L) is neglected in (6)–(8), because the mutual coupling between the two coils (M) is usually very small [1]. In this series-parallel LC tank combination, either L_P or L_S can be used as the transmitter coil, which is the case in Fig. 9(b) and (c), respectively, with their circuit parameters listed in Table I. It is obvious from a comparison between Figs. 9(b2), (c2), and 8(a), (b) that L_P and L_S are more suitable for 5 and 2.5 Mbps, respectively. To have a symmetrical frequency response across the receiver coil, C_r can be chosen such that $C_{in} + C_r$ and L_r resonate at f_r in (6). The time-domain waveforms of V_r in Fig. 9(b3) and (c3) show that the carrier frequency switches immediately with minor residual

TABLE I
CIRCUIT PARAMETERS OF WIRELESS LINK

Parameter	Value	Comment
f_i	5 MHz	Carrier frequency for logic '1'
f_0	10 MHz	Carrier frequency for logic '0'
C_S	0.5 nF	Series tank capacitor
L_S	1 μ H	Series tank inductor
N_S	7	Series inductor turns
D_S	20 mm	Series inductor diameter
C_P	1 nF	Parallel tank capacitor
L_P	0.5 μ H	Parallel tank inductor
N_P	3	Parallel inductor turns
D_P	30 mm	Parallel inductor diameter
$C_{in} + C_r$	50 pF	Receiver tank capacitor
L_r *	7.36 μ H	Receiver tank inductor
N_r	13	Receiver inductor turns
D_r	12 mm	Receiver inductor diameter
T_r	2 mm	Receiver inductor thickness
d_r **	5 mm	Coils relative distance
M	100 nH	Mutual inductance between Coils
R_L	1 k Ω	Biomedical implant loading
R_S	50 Ω	Power amplifier output resistance

* The receiver coil is wound on a ferrite core (Fair Rite material #61).

** From the upper surface of the lower coil to the lower surface of the upper coil with no lateral or angular misalignment.

ringing, which is small enough not to distort the received waveform in a way that the FSK demodulator cannot detect the correct data bit [compare with V_r in Fig. 9(a3)]. Fig. 9(b3) and (c3) also shows that f_0 and f_1 are suppressed in V_{PA} , and there are only spikes at the frequency switching points due to the other unsuppressed frequency components that become significant at these points. This suppression reduces the amplifier power dissipation by reducing its output voltage, thus improving the overall power-transmission efficiency.

Yet, another method to establish a wideband inductive link for the aforementioned FSK demodulators is to setup a dual-frequency, class-E FSK transmitter, which is introduced in [28].

V. MEASUREMENT RESULTS

The RDFS and DFSK demodulator was implemented in an in-house 3- μ m, 1M/2P BiCMOS process [29] to be integrated on microelectrode arrays that were fabricated in the same process [23]. Despite high process-dependent parameter variations in a multipurpose academic facility, satisfactory results were achieved, and reported in [25]. The RDFS and DFSK demodulators, along with an integrated full-wave rectifier [30], were included in a prototype chip for a wireless stimulating microsystem, and fabricated in the AMI 1.5- μ m, 2M/2P standard CMOS process, which is shown in Fig. 10, [26], [27]. With a 5-V supply, the on-chip ring-oscillator generates $f_{TB} = 50.5$ MHz, which is very close to the target value of 49 MHz. According to (4), with this f_{TB} value, the DFSK demodulator works with FSK carriers from 3.2/6.4 MHz to 6.3/12.6 MHz. Therefore, even though the chip was designed for a 4/8 MHz carrier, as discussed in Section III-B and simulated in Fig. 7, a 5/10-MHz carrier was used in measurements to achieve a higher data rate.

To measure the wideband inductive link characteristics, the circuit shown in Fig. 9(c1) was utilized with the power amplifier replaced with a function generator (Agilent 33 250 A), generating a 20-V_{p-p} sinusoid. To measure the generator output current (I_{PA}), a 10- Ω resistor was added in series with the generator 50- Ω output, and V_{PA} was measured after this resistor

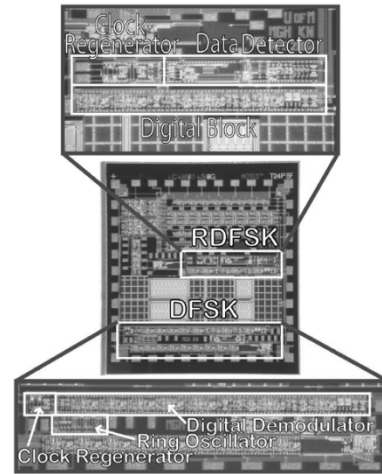


Fig. 10. Die micrograph of the RDFS and DFSK demodulators, implemented in a prototype chip [26], [27].

($R_S = 60 \Omega$). The wideband inductive link was set up according to the specifications listed in Table I, with the series-parallel LC tank combination connected to the generator by a pair of short wires. In practice, the effect of longer cables should be considered in calculating L and C values, using the transmission line theory [31]. Fig. 11(a) shows the generator output voltage and current (V_{PA} , I_{PA}) as well as the voltages across transmitter (L_S) and receiver (L_r) coils (V_t , V_r) versus carrier frequency. The transmitter output power $P_t = V_{PA} \times I_{PA} \times \cos(\varphi)/8$, where φ is the phase delay between V_{PA} and I_{PA} , and the resistive load (R_L) received power $P_r = V_r^2/8R_L$ were calculated, and shown in Fig. 11(b) along with the inductive link efficiency, $\eta\% = 100P_r/P_t$, all in the frequency domain. A comparison between Fig. 8(b), V_r , and η spectrums in Fig. 11(a) and (b), and simulated V_r waveform in Fig. 9(c3) shows that the designed wideband inductive link is capable of transmitting the significant frequency components of the proposed FSK carrier with the gain and power efficiency that is about 25%–50% of the narrow-band methods [1]–[5], while minimizing distortion and ISI. It is also important to note that in the near field, the gain and efficiency of the inductive link are strong functions of the relative coils distance. Fig. 11(c) shows measured V_r and η at 5 and 10 MHz versus d_r in 2–14 mm range.

To evaluate the overall performance of the DFSK demodulator and the wireless link, a square-shaped digital FSK signal was generated on a PC platform, based on the proposed FSK protocol, using a high-speed digital I/O card (National Instruments DAQ-6534) in LabView environment. The digital FSK signal, which has a 2.5-V dc component, passes through a dc-level adjustment circuit and bandpass filter (0.01–10 MHz), which reject its dc and high frequency components, and turn it into a bipolar sinusoidal FSK signal, before being amplified by a wideband power amplifier (Amplifier Research 25A250A). The amplified FSK carrier is then transmitted through the inductive link setup. L_r , which can be inductively coupled to either L_P or L_S , picks up the FSK carrier, and applies it to the rectifier and demodulator blocks. Depending on d_r , the power amplifier gain was adjusted such that the on-chip rectifier dc output, filtered by an off-chip 10-nF capacitor, supplied the

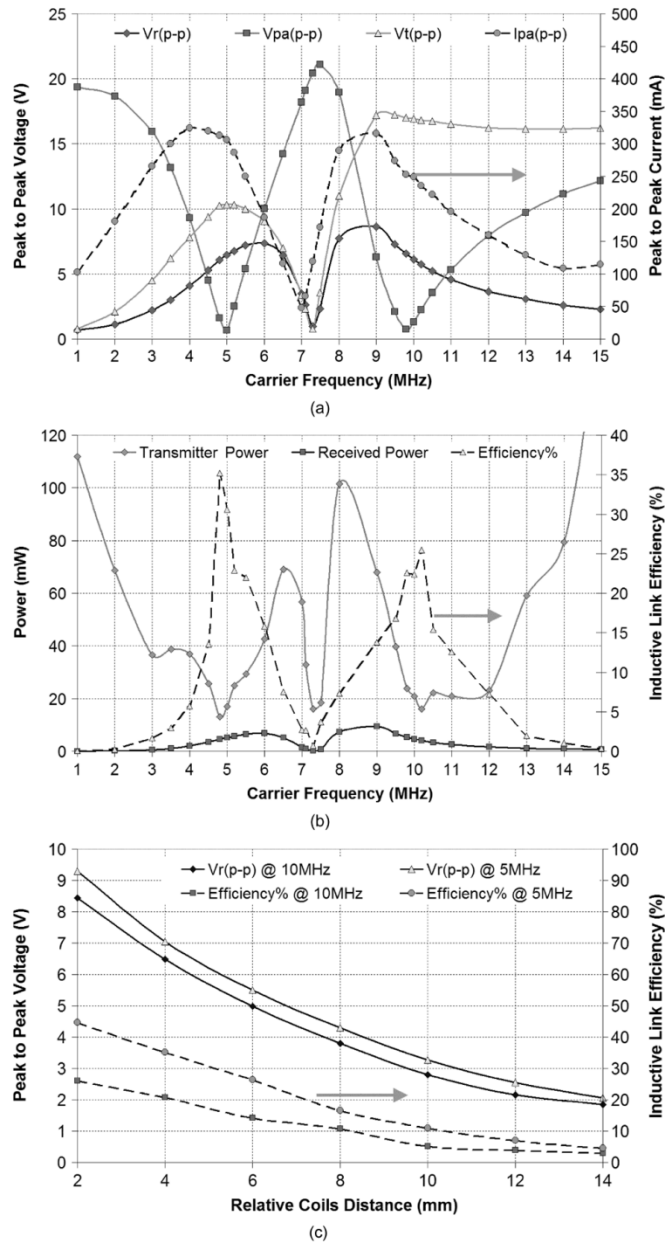


Fig. 11. Wideband inductive link measured characteristics. (a) V_r : Voltage across L_r , V_{PA} : Voltage across series-parallel LC tank combination, V_t : Voltage across L_S , and I_{PA} : Current through LC tank combination versus carrier frequency. (b) Transmitter power, received power, and inductive link efficiency versus carrier frequency. (c) V_r and inductive link efficiency at 5 and 10 MHz versus relative L_S and L_r coils distance.

entire chip at 5 V. In Fig. 12, the received FSK carrier, measured differentially across the $L_r C_r$ -tank, is shown on the 3 lower traces ($\sim 30 V_{p-p}$). The bandpass filter on the transmitter side attenuates f_0 slightly more than f_1 , which causes some amplitude modulation on the received carrier, when the inductive link spectrum is quite symmetrical, as in Fig. 9(b) and (c). This amplitude modulation can be eliminated in practice by tuning the $L_r C_r$ -tank resonance frequency closer to f_0 , as shown in Fig. 11(a). Even though a maximum data rate of $f_1 = 5$ Mbps can be transmitted by a 5/10-MHz carrier, according to the proposed FSK protocol, the practical inductive link bandwidth was not enough for a full-speed data rate with high enough BER.

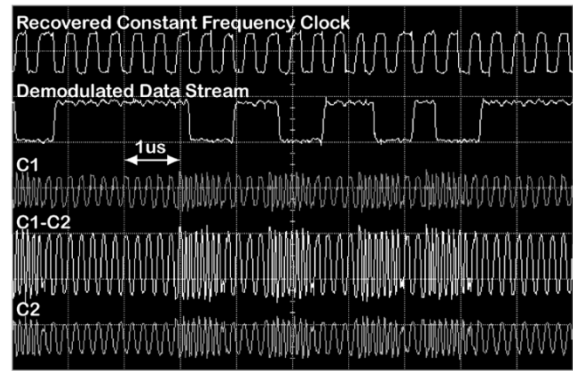


Fig. 12. Measured waveforms of the DFSK at 2.5 Mbps with f_0 and f_1 equal to 10 and 5 MHz, respectively. From top: *Clock-Out*, *Data-Out* [5 V/div], and single ended (C_1 , C_2) and differential (C_1-C_2) carrier voltage at across the receiver $L_r C_r$ tank circuit [20 V/div].

TABLE II
MEASURED RESULTS AND SPECIFICATIONS OF FSK DEMODULATOR CIRCUITS

Demodulation Technique	FDFSK	RDFSK	DFSK
Process technology	UM 3- μ m	AMI 1.5- μ m	AMI 1.5- μ m
Die size (mm ²)	2.0 \times 2.0	2.2 \times 2.2	2.2 \times 2.2
Circuit area (mm ²)	0.67	0.41	0.29
Max simulated data-rate (Mbps)*	2.5	4	4
Max measured data-rate (Mbps)	1	1.5	2.5*
C (pF)	1.0 & 2.0	1.2	N/A
I_C (μ A)	20 & 33	40	N/A
V_{ref} (V)	N/A	1.26	N/A
Time-base clock (MHz)	N/A	N/A	50.5
Counter width (n)	N/A	N/A	3
Bit error rate at 2.5 Mbps	-	-	10^{-5}
Demodulator supply voltage (V)	5	5	5
Transmitter output voltage (V_{p-p})	100	100	100
Power consumption at 5 V (mW)	0.55	0.45	0.38

* Depending on the fabrication process parameters and rules.
Limited by the wireless link bandwidth.

Therefore, the data rate was reduced to 2.5 Mbps by repeating every bit twice, as shown in Fig. 8(b), and the receiver coil was coupled to L_S to achieve a BER = 10^{-5} . The two upper traces in Fig. 12 show the recovered clock (*Clock-Out*) and demodulated serial data bit-stream (*Data-Out*) at 2.5 MHz and 2.5 Mbps, respectively. To measure the BER, several million bits were generated, transmitted across the wireless link, and recorded on a different computer, which was connected to the DFSK demodulator, for at least five times. The recorded serial data bit-streams were then compared to the original, off-line, to calculate the average BER. To the authors' knowledge, this is the fastest data rate ever reported in inductively coupled wireless applications [5]–[13].

Table II compares the measured results and specifications of the three demodulator circuits that were discussed in Section III. All these circuits are designed for the highest data rate achievable in their fabrication processes, without optimization in terms of power or chip area consumption. With this criterion, the DFSK circuit seems to offer the best performance. However, it should be noted that with a different set of design criteria, the optimal choice might be different. For example, if a high data rate to carrier frequency ratio is sought by using a carrier frequency in the 100-kHz range, then I_C in Fig. 4(b) can be much smaller, and the RDFSK demodulator would be the most power-efficient solution. On the other hand, the FDFSK method is the most robust against process variations because of its differential nature, at the expense of more power consumption.

VI. SUMMARY

We have developed a high-rate phase-coherent FSK modulation protocol, a wideband inductive link, and three FSK demodulator circuits for wireless operation of the inductively powered devices in need of high data rates, such as stimulating microelectrode arrays with over 1000 stimulating sites. The phase-coherent FSK modulation/demodulation technique, which has several advantages over the typical ASK method, can also be used in other applications such as RFID tags and smartcards by adding a mechanism for back telemetry. A wideband inductive link is designed by using a series-parallel LC tank combination, between a pair of loosely coupled coils to receive the FSK carrier signal across the receiver coil without significant distortion. In the demodulator circuit, a serial data bit-stream and a constant frequency clock are extracted from the FSK carrier, which can be in the 1–25 MHz range, and also powers the chip after being rectified. The FDFSK demodulator is fabricated in the 1M/2P, 3- μm UM-BiCMOS process, occupying 0.67 mm². The RDFSK and DFSK demodulators are fabricated in the AMI 2M/2P, 1.5- μm standard CMOS process, occupying 0.41 and 0.29 mm², respectively. The measurement and simulation results, which are summarized in Table II, suggest that the DFSK demodulator is the best choice for achieving the highest data rate. However, with different design criteria, the analog approaches might be favorable based on the system requirements. By migrating to newer processes with smaller feature size, while using the proposed techniques, the main data rate limiting factor seems to be the inductive link bandwidth, and not the speed of the demodulator circuitry. It is also possible to narrow down the required inductive link bandwidth by choosing f_0 and f_1 closer to one another at the expense of a more complicated synchronization scheme.

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